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Hardware Architectures of Visible Light Communication Transmitter and Receiver for Beacon-based Indoor Positioning Systems

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Abstract– **High-speed applications of Visible Light Communications have been presented recently in which response times of photodiode-based VLC receivers are critical points. Typical VLC receiver routines, such as soft-decoding of run-length limited (RLL) codes and Forward Error Correction (FEC) codes was purely processed on embedded firmware, and potentially cause bottleneck at the receiver. To speed up the performance of receivers, ASIC-based VLC receiver could be the solution. Unfortunately, recent works on soft-decoding of RLL and FEC have shown that they are bulky and time-consuming computations. This causes hardware implementation of VLC receivers becomes heavy and unrealistic. In this paper, we introduce a compact Polar-code-based VLC receivers. in which flicker mitigation of the system can be guaranteed even without RLL codes. In particular, we utilized the centralized bit-probability distribution of a pre-scrambler and a Polar encoder to create a non-RLL flicker mitigation solution. At the receiver, a 3-bit soft-decision filter was implemented to analyze signals received from the VLC channel to extract log-likelihood ratio (LLR) values and feed them to the Polar decoder. Therefore, the proposed receiver could exploit the soft-decoding of the Polar decoder to improve the error-correction performance of the system. Due to the non-RLL characteristic, the receiver has a preeminent code-rate and a reduced complexity compared with RLL-based receivers. We present the proposed VLC receiver along with a novel very-large-scale integration (VLSI) architecture, and a synthesis of our design using FPGA/ASIC synthesis tools.**

Keywords– **Polar Code, Flicker Mitigation, Run-length Limited (RLL), Visible Light Communication (VLC), Receiver.**

1 Introduction

1.1 VLC-beacon-based Indoor Positioning Systems (IPS)

VLC simultaneously provides both illumination and communication services. Specifically, VLC systems currently utilize visible light for communication that occupy the 380nm-750nm spectrum [1, 2]. Some modulation schemes have been introduced for VLC systems, e.g. Variable Pulse Position Modulation (VPPM), On-off Keying (OOK), or Orthogonal Frequency Division Multiplexing (OFDM) and so on [2, 3]. The VLC transmitter modulates the digital information to light signals through a transmit (TX) front-end and a light-emitting diode (LED).

Generally, indoor localization applications which show users' locations in indoor buildings are getting more attentions from researchers and industry in recent years [3, 4]. Several statistics show that human spend almost 80% time of a day indoor where global positioning systems (GPS) could not work [4, 5]. Accordingly, indoor localization is the key to open a wide range of location-based service (LBS) applications. Indeed, mobile indoor positioning in retail is estimated up to $5 billion in 2018 [3]. Current approaches in indoor positioning which are often based on Wi-Fi, Ultra-wideband (UWB), Radio-Frequency Identification (RFID), or other RF wireless techniques [3]. These approaches often meet problems related to high cost of installation and management; or can not be used in Radio Frequency (RF) banned areas such as hospitals, planes or gas stations [3]. VLC-based indoor positioning solutions have promising characteristics such as low cost, high security, high spatial reuse, low co-channel interference, high-precision and so on [3, 5]. VLC-based solutions, therefore are considered widely as suitable candidates for indoor positioning. In VLC-beacon-based indoor localization systems, unique ID information are transmitted from VLC-LED bulbs for purposes such as identifying objects and locations [6]. Furthermore, beacon-based frames have been introduced in some publications with the sizes of 158-bit [6], 56-bit [7] or 34 symbols (0.96ms) [8]. We found that the 158-bit beacon-based frame which is defined by Standard of Japan Electronics and Information Technology Industries Association (JEITA) [2, 8] should be considered because this work is confirmed by an association. Particularly, the structure of the JEITA's beacon-based frame includes three parts: start of frame (SOF), payload, and the end of frame (EOF). The SOF includes 6-bit preamble indicating the beginning of the frame, and another 8-bit defines the frame type. The payload includes 128-bit ID data. Finally, 16-bit

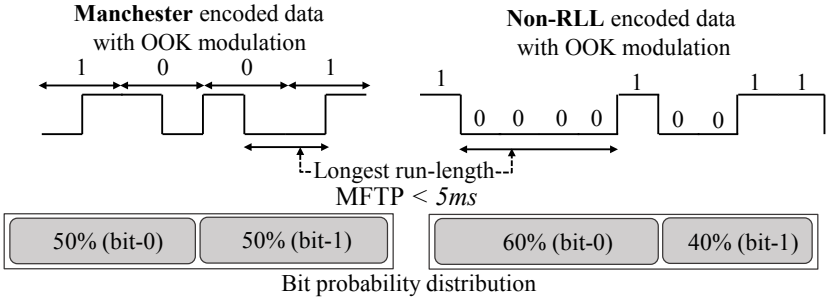

Figure 1. Run-length, bit probability distribution and flicker mitigation.

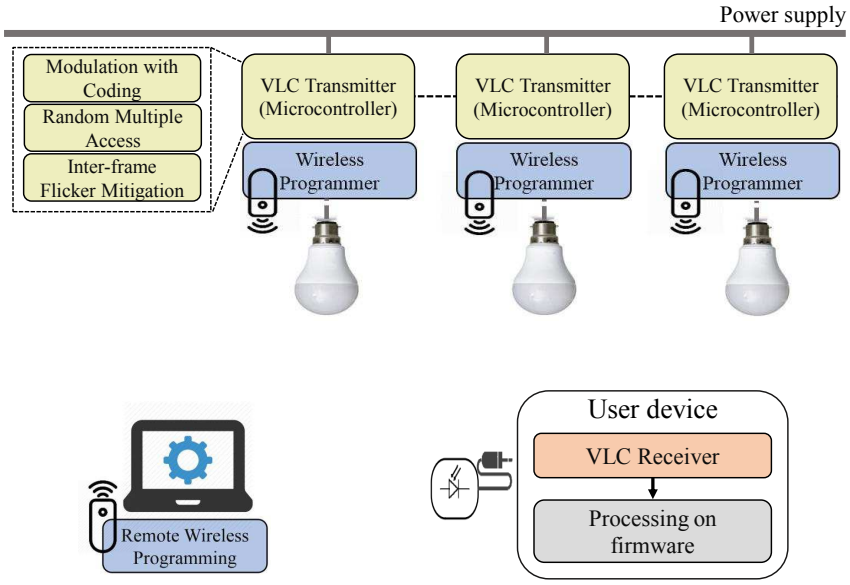

Figure 2. An example of a VLC-based indoor positioning system.

cyclic redundancy is reserved for error correction [6]. There is one fact that beacon broadcasting of VLC-based indoor localization systems does not require a high-speed link. Therefore, throughout this paper, we consider the OOK modulation because of its simplicity and easy implementation. Also, we favor in setting a low frequency for the proposed system to evaluate its performance.

1.2 Flicker Mitigation Problem

The brightness and stability of the light are strongly affected by the distribution of the 1's and 0's in the data frames. RLL coding is indispensable to avoid LED's flicker and guarantee the direct current (DC) balance in visible light communication systems. Therefore, many DC-balance solutions are introduced to maintain approximately equal numbers of zero and one bits in the data frames. As a result, flicker mitigation which based on DC-balance techniques is considered as one of essential concerns in any VLC systems. Moreover, when the light source is modulated for data communication, run-length of the data codewords should be carefully controlled to mitigate the potential flickers. To avoid flicker, the changes in brightness must be faster than the maximum flickering time period (MFTP), which is defined by the maximum time period that light intensity can change without being perceived by human eyes [9]. In normal cases, a MFTP which is faster than 5 ms is considered safe for a non-flicker guarantee. Figure 1 shows an illustrative example to introduce how run-length and bit probability distribution affect to the flicker of VLC systems in case of light is modulated by OOK method. When data is modulated by Manchester coding, the maximum run-length is limited to 2 while the ratio of bit-0 and bit-1 are always equal in all cases. On the contrary, bit-distribution and run-length of non-RLL cases are arbitrary. Therefore, non-RLL approaches potentially cause flickers which could be recognized at the LED bulbs. As a result, whenever the non-RLL scheme is considered for VLC systems, the run-length and centralized bit probability distribution should be carefully investigated. Also, the lowest transmit frequency that can guarantees flicker mitigation should be considered in such non-RLL OOK VLC systems.

1.3 Why the Hardware Implementation of VLC Transmitter and Receiver is Important?

Figure 2 shows an example of a typical VLC-based indoor localization system in which VLC transmitter's function blocks are mainly processed by a firmware program on a trivial micro-controller. The VLC receiver and positioning algorithm are executed on a firmware program of a user's portable device [7]. Furthermore, an optional part of the VLC transmit (TX) package is

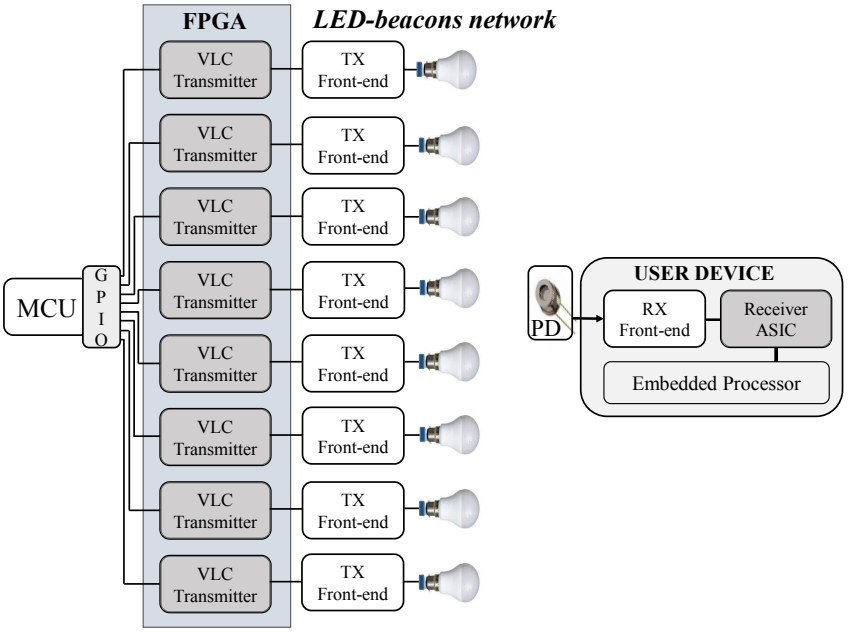

Figure 3. The proposed VLC-LEDs beacons network based on our hardware works.

the wireless programmer which helps configure the firmware on the low-end micro-controller remotely. It can be found that when VLC-based indoor positioning system is applied inside a large building in which hundreds or thousands of VLC-LED bulbs required. In this case, the implementation cost increase linearly because each micro-controller is dedicated for only one VLC-LED anchor [7], or several LEDs [10]. Moreover, each VLC-beacon package takes more space to integrate the programming circuits. On the other hand, if we assume that only one micro-controller is employed to control many VLC-LED beacons and long wires are used for routing to LED bulbs through VLC TX front-ends. As a result, the encoding of FEC and RLL codes is processed sequentially on MCU's firmware before encoded data is feed to numerous of VLC TX beacons. Although FEC encoding or RLL encoding are not time-consuming tasks, however, to deal with a large number of VLC transmitters, this scenario sometimes limits the smooth operation of the VLC-based beacon system in which its time constraints and flicker mitigation must be guaranteed. Moreover, due to the limited capability of the low-end micro-controller, only a few VLC-based beacons are well managed by one micro-controller. Hence, this restricts the scalability of the VLC-based indoor localization systems.

On the contrary, VLC receiver's function blocks which include decoding of RLL and FEC codes are purely processed on user's portable device. However, some soft-decoding RLL and FEC algorithms have been proposed recently in VLC systems [11–14]. These solutions help improve the performance of the VLC receiver; however, they are potentially time-consuming tasks with many complex mathematical computations. Besides, fastidious users always expect real-time responses or for their indoor positioning application. Therefore, VLC soft-decoding receivers or localization algorithms need to be optimized and simplified.

Because of problems mentioned until now, we propose two dedicated hardware implementations for VLC transmitter and receiver. The overview of our proposal is briefly presented in Figure 3. In particular, we have utilized the parallel processing capability of the FPGA to implement VLC transmitters inside an FPGA which connects to many TX front-ends in the LED-beacon network. Specifically, one VLC transmitter hardware executes tasks, for instance, modulation with coding, random multiple access or inter-frame flicker mitigation [7]. Accordingly, ID information of each VLC-LED bulb is processed directly at each VLC transmitter right after the center MCU pushes coarse bits to GPIO ports. Therefore, only one micro-controller is required to monitor all the IDs issued for all LED bulbs. At the user device, the dedicated VLC receiver ASIC is expected to enhance the processing time of soft-decoding of FEC or RLL codes, which contains heavy mathematic computations e.g. multiplication, exponential, logarithm functions and so on [12, 14]. Hence, VLC-based indoor localization systems can be operated smoothly without recognizable delays. In this paper, we introduce a couple of hardware implementations with VLSI architectures of the proposed compact VLC transmitter/receiver; in which essential problems related to flicker mitigation and soft-decoding of RLL and FEC are clearly discussed.

2 Related Works on Flicker Mitigation and DC-balance

Table I summarizes proposals related to FEC and flicker mitigation for VLC. The conventional solution is defined in the IEEE 802.15.7 standard, which employs

Table I
Overview of FEC Algorithms and Flicker Mitigation Solutions for VLC

FEC solution	Flicker mitigation
RS, CC [15]	Hard-RLL
Multi-RS hard-decoding [16]	Hard-RLL
LDPC [17]	Hard-RLL
RS soft-decoding [11, 12]	Soft-RLL
Polar code [13, 14, 18]	Soft-RLL
Irregular CC [19]	Unity-Rate Code
Irregular CC [20]	Unary-Rate Code
Reed-Muller [21]	Modified original code
Turbo code [22]	Puncture + Scrambling
Fountain code [23]	Scrambling
Convolutional code, Viterbi [24]	Enhanced Miller code
Polar code (N=2048) [9]	Flicker-free
Proposed method (K=158, N=256) (JEITA's beacon frame size)	Flicker-free

Table II
Code-Rate Comparison of Non-RLL and RLL Solutions

Code	Code-rate
Manchester	1/2
FM0/FM1	1/2
Conventional Miller [24]	1/2
eMiller [24]	1/2
4B6B	0.67
8B10B	0.8
non-RLL (our work)	1 (No changed)

Reed-Solomon (RS) codes, Convolutional Codes (CC) and RLL codes with hard-decoding of RLL codes (hard-RLL) [15]. However, hard-RLL methods of inner RLL codes limit to hard-decoding of outer FEC codes [15, 16, 21]; consequently, the error-correction performance of the entire VLC system is restricted. Recently, soft-decoding RLL (soft-RLL) solutions have been proposed in [11–14]. These techniques permit soft-decoding FEC algorithms to be applied to improve the bit-error-rate (BER) performance of the VLC system, but they also require heavy computational efforts, with many additions and multiplications [25].

Zunaira *et al.* have proposed replacing the classic RLL codes with a recursive Unity-Rate Code (URC) or an Unary-Code as the inner code, and a 17-subcode IRregular Convolutional Code (IRCC) is selected for the outer code [19, 20, 26]. Although these methods can achieve different dimming levels with good BER performances; however, the system latency is increased with the iterative-decoding schemes. In addition, the reported codeword length is rarely long, which ranges from 1000 to 5000 bits, reduces the compatibility of this proposal to VLC-based beacon systems [6, 7] in which beacon-based frame sizes are always small. As an alternative approach, Kim *et al.* have proposed a coding scheme based on modified Reed-Muller (RM) codes [21]. Although this method can guarantee DC balance at exactly 50%, it has the inherent drawbacks of a deducted code rate and an inferior error-correction performance compared with turbo codes, low-density parity-check (LDPC) codes or polar codes. In addition, Lee and Kwon have proposed the use of puncturing and pseudo-noise sequence scrambling with compensation symbols (CS) [22]. This proposal can achieve very good BER performance; however, puncturing with CSs will lead to redundant bits in the messages, thereby reducing the transmission efficiency. Another coding scheme based on the fountain code, which has greatly improved the transmission efficiency, is mentioned in [23]. However, this scheme requires feedback information and thus is not suitable for broadcasting scenarios in VLC-based beacon systems. Xuanxuan Lu *et al.* have reported a new class of enhanced Miller codes, termed eMiller codes which is a class of RLL codes known for high-bandwidth efficiency [24]. Besides, she also proposed an improved version of Viterbi algorithm, termed *mnVA* to further enhance the performance of her proposed eMiller code. It can be seen from her simulation results that eMiller helps improve the performance of the whole VLC system; and this code seems to be a promising candidate for VLC applications. However, we have found two main drawbacks of this approach are the unoptimized code-rate = 1/2 of the eMiller code (Table II), and an increasing in computational complexity.

Advantages of Polar code are exploited deeply together with soft-decoding of RLL codes have been introduced at [13, 14]. According to these publications, Manchester and 4B6B codes are used as RLL solutions for the VLC system. As a result, their BER performances have been improved remarkably with a flexibility of Polar code's code-rate. However, we found that the code-rate = 1/2 of Manchester code, or code-rate = 0.67 of 4B6B (summarized at the Table II) are also not the best optimization solution for channel efficiency enhancement, if compared with non-RLL approaches. Fang *et al.* have recently proposed a non-RLL polar-code-based solution for dimmable VLC systems [9]. This approach has shown promising results in weight distribution and run-length distribution. Moreover, this solution also shows an improved transmission efficiency while achieving a high coding gain compared with RS and LDPC codes. We have found that this solution can overcome most of the drawbacks of the related works mentioned until now. Specifically, it offers the non-iterative decoding with a low-complexity. Also, it has a flexible code-rate, and a high BER performance without requiring any feedback information. However, we found that the biggest obstacle of this proposal is the equal probabilities of short runs of 1's and 0's can only be achieved with a long codeword length; as chosen to be $N = 2048$. Indeed, long data frames rarely be applied in low-throughput VLC systems, for instances, VLC-based beacon ones [6, 7]. It can be found that the non-RLL solution based only on a polar encoder [9]

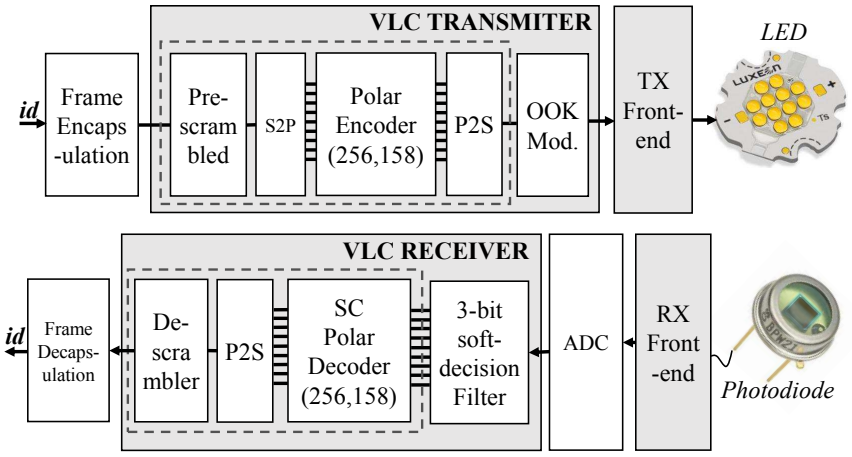

Figure 4. Block diagram of the proposed VLC transmitter/receiver hardware architecture.

might not be applicable in such VLC-based beacon systems because DC balance is not guaranteed for short data frames.

In the later parts of this paper, we point out the unsolved problems of non-RLL flicker mitigation in VLC-based beacon systems. Additionally, as mentioned in Section 1.3, we introduce a couple of non-RLL beacon-based VLC transmitter and receiver and their VLSI architectures for the first time. In summary, our contributions include:

1) First discussion on the importance of FPGA and ASIC implementations of VLC transmitters and receivers in VLC-based beacon systems (Section 1.3)
2) A non-RLL flicker mitigation method based on a prescrambled Polar encoder (Section 3).
3) Two proposed hardware architectures of beacon-based VLC transmitter and receiver (Section 4).
4) A 3-bit soft-decision filter which can support soft-decoding of FEC decoders in real prototypes of VLC receivers (Section 4.2.1).

3 Flicker Mitigation based on a Non-RLL Prescrambled Polar Encoder

It follows from the Section 2, due to the small size of beacon-based data frames, a non-RLL DC-balance solution which dedicated for the VLC-based beacon systems seems still to be an unsolved problem. In this section, we introduce a non-RLL flicker mitigation solution which is designed for VLC-based beacon systems. Particularly, our flicker mitigation solution is the combination of a simple pre-scrambler placed at the outer code, with a (256;158) polar encoder placed at a inner code's position. Figure 4 briefly introduces our proposal in style of block diagram.

Table II summarizes a code-rate comparison of RLL and non-RLL solutions. It can be noticed that non-RLL solutions keep the system rate unchanged while removing the heaviness of RLL encode/decode blocks. Furthermore, FEC decoders also inherit from the removing RLL codes because soft-decoding of them can be implemented without difficulties in achieving LLR values. However, DC-balance and run-length should be controlled strictly in such non-RLL VLC systems.

In a digital transmission system, a data scrambler plays an important role because it causes energy to be spread more uniformly. At the transmitter, a pseudo-random cipher sequence is modulo-2 added to the data sequence to produce a scrambled data sequence.

Describe the generating polynomial $P(x)$ as:

$$P(x) = \sum_{q=0}^{N} c_q.x^q, \tag{1}$$

where $c_0 = 1$ and is equal 0 or 1 for other indexes.

We have found that the output bit probability distributions of pre-scramblers in different generating polynomials seem to differ slightly. Therefore, we propose a simple generating polynomial presented in (2) to reduce the number of shift registers required for a pre-scrambler.

$$P(x) = x^4 + x^3 + 1 \tag{2}$$

Meanwhile, polar codes can be classified into two types: non-systematic and systematic codes. Typically, a polar code is specified by a triple consisting of three parameters: *(N, K, I)*, where N is the codeword length, K is the message length, and I is the set of information bit indices. Let d be a vector of N bits, including information bits. The generator matrix is defined as $G = (F^{\otimes n})_I$. Then, given a scrambled message u of K bits in length, a codeword x is generated as given in (3).

$$x = u.G = d.F^{\otimes n} \tag{3}$$

A Polar encoder is formed of many layers of XOR gates, with a complexity of $\frac{N}{2}\log_2 N$ XORs. There is one fact that systematic polar codes were introduced to achieve better error-correction performances compared with non-systematic codes [27]. However, due to the information bits transparently appear as a part of the codeword, we have found that the output bit-probability distribution of a systematic Polar encoder (SPE) is not well centralized. On the other hand, the output bit probability distribution of an non-systematic Polar encoder (NSPE) naturally becomes centralized

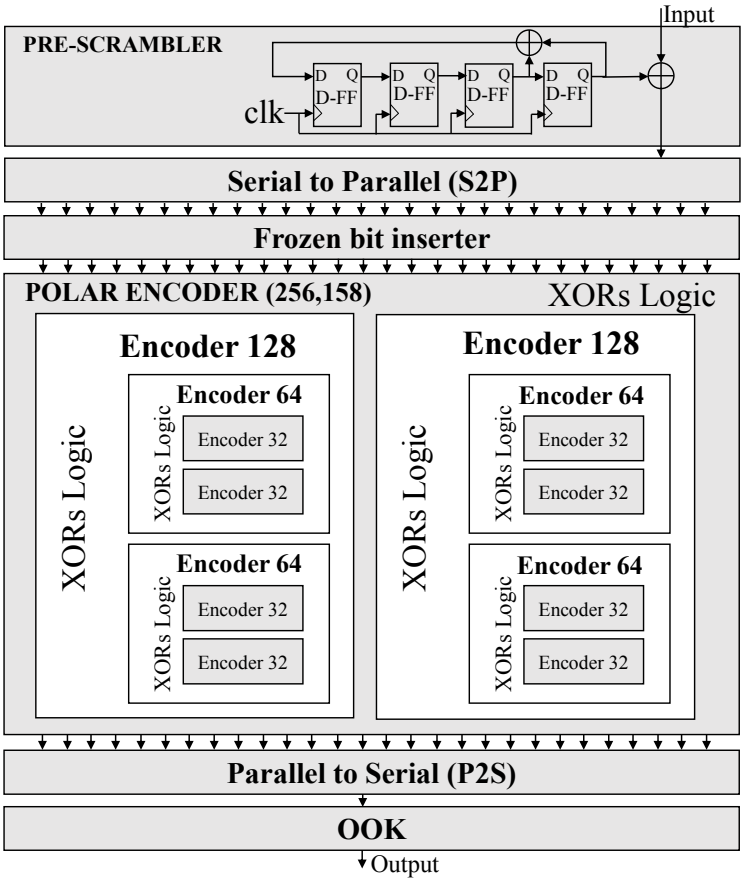

Figure 5. The hardware architecture of proposed non-RLL VLC transmitter.

approximately 50% 1's and 50% 0's when the codeword length is long enough [9].

In summary, we have selected the Polar code as the main FEC scheme for our VLC-based transmitter/receiver due to several reasons:

1) The encoder's output bit probability distribution is naturally centralized when long codewords are applied in the system.
2) Unusual code rates are supported. Specifically, a (256;158) polar code, which has a code rate of 0.617, is suitable for a beacon-based frame size of K=158.
3) High error-correction performance can be achieved with a low hardware complexity [28].
4) The inherently short run lengths of a polar encoder can be useful in mitigating the lighting flicker [9].

A pre-scrambler can help to ensure the fast convergence of the output probability distribution of an inner (256;158) Polar encoder. As a result, DC balance in a VLC-based beacon system can be guaranteed by the proposed transmitter depicted in Figure 5.

4 Hardware Architecture of the Proposed VLC Transmitter and Receiver

4.1 Hardware Architecture of the VLC Transmitter

Block diagram of the proposed VLC transmitter is shown in Figure 5. As mentioned in Section 2, it seems that Polar code is an optimal candidate for a FEC solution in VLC receiver [9, 14]. In Section 3, we have also introduced a pre-scrambled Polar encoder as a non-RLL flicker mitigation in case of beacon-sized codewords which defined by JEITA are applied in the VLC-based beacon systems. In fact, the IEEE 802.15.7 standard has stated that Reed-Solomon (RS) and convolutional codes are preferred over low density parity check (LDPC) codes in order to support short data frames, hard-decoding with low complexity [15]. We found that flexible code-rates of the Polar code can support any sizes of data frames [27]. Also, its soft-decision decoding can improve the reliability of the VLC systems compared with RS and convolutional codes. Moreover, the inherent low-complexity characteristic of Polar code's encoding and Successive-Cancellation (SC) decoding is suitable for being applied in VLC receivers.

Regarding the proposed VLC transmitter described in Figure 4 and Figure 5. Firstly, 128-bit ID information data is wrapped by a frame encapsulation procedure to form a 158-bit beacon-based frame [6]. Next, the 158-bit frame is scrambled by a pre-scrambler. Due to a simple generating polynomial (2) is applied, only four registers and one XOR gate are required to create a pre-scrambler. The frozen bit inserter feeds $N - K$ frozen bits to different positions in a 256-bit data frame. Particularly, if the JEITA's 158-bit beacon-based frame is applied, 98 frozen bits are inserted at positions defined by the construction algorithm of Polar code.

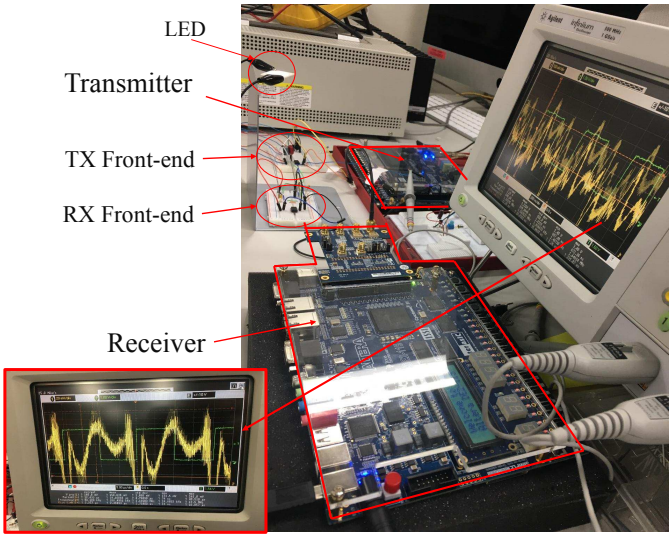

Figure 6. Distorted received signals due to the bad channel settings.

After frozen bits are inserted, the pre-scrambled 256-bit frame is encoded by a Polar encoder (256;158) to create a bit stream in which the DC-balance can be guaranteed without any RLL codes. Regarding the Polar encoder, we have implemented a recursive combinational architecture for the Polar encoder, in which 2^N-code-length encoders are created by $N/2$ XOR gates and two 2^{N-1}-code-length encoders which were depicted in Figure 5. Due to the block encoding characteristic of Polar encoder, the Serial-to-Parallel (S2P) block is implemented to prepare the pre-scrambled serial bit-stream to a 256-bit register. This register is the input register of Polar encoder. Also, Parallel-to-Serial (P2S) block converts parallel Polar encoded bits to serial bit stream before being modulated by the OOK block. Finally, the VLC TX front-end converts the OOK-modulated signals to light signals and broadcast them to the air. Specifically, we have also assembled a VLC TX front-end that successfully transmit information through a normal 5V LED with a transmit frequency up to 2.5 Mhz.

4.2 Hardware Architecture of the VLC Receiver

4.2.1 3-bit Soft-Decision Filter: Figure 6 shows our FPGA-based VLC demonstration system in which distorted signals are received at the VLC RX front-end, then it is displayed on the oscilloscope. Specifically, we have found that distortions appear in two experimental scenarios. Firstly, when the transmit frequency is higher than the maximum frequency that RX front-end can receive. Secondly, when the distance between TX LED and RX front-end increases in space. Also, distortions of the received signals also appear with shrunken peak-to-peak voltages (*Vpp*). Distorted received signals are usually the cases cause reliability of the VLC system deducted because hard-decoding of RLL and FEC are often the default selections in most VLC receivers [15]. In this paper, we introduce a 3-bit soft-decision filter which is implemented at VLC receiver to support soft-decoding of RLL and FEC decoders in real VLC receiver prototypes.

Specifically, in the case of VLC AWGN channel, a sequence of the *LLR* values which is necessary for soft-decoding of FEC decoder, are expressed by Equation (4).

$$LLR(y_i) = \ln \frac{P(x_i = 0|y_i)}{P(x_i = 1|y_i)}, \tag{4}$$

where y_i is the received sample and the conditional probability is generally calculated as Equation (5).

$$P(x_i|y_i = \Delta) = \frac{1}{\sqrt{2\pi\sigma_\Delta^2}} e^{-\frac{(y_i-\mu_\Delta)^2}{2\sigma_\Delta^2}}, \tag{5}$$

where μ_Δ and σ_Δ are the mean value and standard deviation for $\Delta = 0, 1$. However, when making real prototype of soft-decoding VLC receiver, we found that it is unfeasible in estimating the LLRs using such Equation (4) and Equation (5) due to μ_Δ and σ_Δ can not be estimated in real optical wireless channels. Therefore, in this paper, we propose applying a soft-decision filter which is first introduced in optical communication systems for our VLC receiver prototype [29].

Figure 7 shows the proposed hardware architecture of 3-bit decision filter that we have implemented. Firstly, an analog-to-digital converter (ADC) converts analog signals received from the RX front-end to digital signals. The 3-bit soft-decision filter analyses these digital signals and calculate LLR values to feed to soft-decoding Polar decoder. The soft-decision filter includes 2^{N-1} decision thresholds to compare with the incoming received signal, where N is the number of quantization bits. Previous research on soft-decision filter in optical communication systems has shown that 3-bit soft decision was the optimum solution [29, 30]. In the case of N=3 for 3-bit soft decision, we established seven threshold voltages from V_{t+3} to V_{t-3} which are calculated from equations given in Equation (6). We have defined a mapping table with output LLR values are carefully chosen from training simulation results on MATLAB. Table III shows ranges of comparison and their output LLR values. The sequence of 9-bit

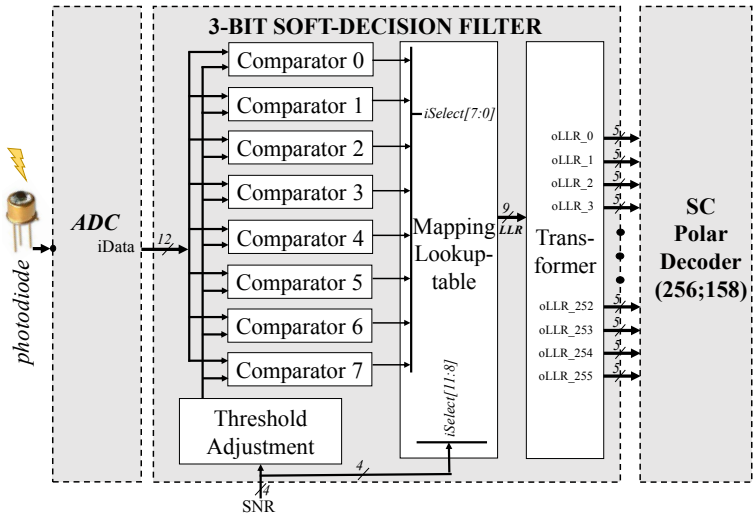

Figure 7. Hardware architecture of the 3-bit soft-decision filter.

LLR results of mapping lookup-table are buffered and quantized by a block named *Transformer*, before passing them to the Polar decoder.

$$
\begin{aligned}
V_t &= \frac{V_{peak+} + V_{peak-}}{2} \\
V_{t-1} &= V_t - \frac{V_{peak+} - V_t}{4} \\
V_{t-2} &= V_t - 2\frac{V_{peak+} - V_t}{4} \\
V_{t-3} &= V_t - 3\frac{V_{peak+} - V_t}{4} \\
V_{t+1} &= V_t + \frac{V_{peak+} - V_t}{4} \\
V_{t+2} &= V_t + 2\frac{V_{peak+} - V_t}{4} \\
V_{t+3} &= V_t + 3\frac{V_{peak+} - V_t}{4}
\end{aligned}
\tag{6}
$$

4.2.2 Successive cancellation (SC) Polar decoder and descrambler: Figure 8 shows the proposed hardware architecture of our non-RLL VLC receiver. Firstly, as explained in Section 4.2.1, the proposed 3-bit soft-decision filter enables applying a soft-decoding Polar decoder at the VLC receiver to increase the reliability of the system. Indeed, the soft-decision filter passes 256 LLR values to the parallel inputs of the SC polar decoder. Compared with conventional architectures of the Polar decoder, our implemented polar decoder (256;158) has three unusual features. Firstly, 8 layers of processing elements (PEs) are purely processed by the combinational logic, because we have removed all intermediate registers to reduce the decoding latency. Secondly, the last stage's PE is modified to output two decoded information bits every each clock cycle. These two modified points have been presented in our previous work [28]. Thirdly, we have implemented a partial sums generator (PSG) based on Polar encoders with various code-length sizes, and integrate the PSG into the scheduling control block of the SC Polar decoder. The decoded data is converted to serial form and is descrambled by a descrambler. Finally, the frame decapsulation block removes the SOF and EOF fields to extract the ID data.

Table III
The Mapping Table of 3-bit Soft-Decision Filter

Comparator	Range	Output LLR values
0	$[V_{peak+}\ ;\ V_{t+3}]$	1.2017
1	$[V_{t+3}\ ;\ V_{t+2}]$	0.3630
2	$[V_{t+2}\ ;\ V_{t+1}]$	0.2185
3	$[V_{t+1}\ ;\ V_t]$	0.0656
4	$[V_t\ ;\ V_{t-1}]$	-0.0702
5	$[V_{t-1}\ ;\ V_{t-2}]$	-0.2116
6	$[V_{t-2}\ ;\ V_{t-3}]$	-0.3547
7	$[V_{t-3}\ ;\ V_{peak-}]$	-1.1943

5 Evaluation and Experimental Results

5.1 Flicker Mitigation Results

In the previous non-RLL solution work based only on a polar encoder [9], the authors have demonstrated the fluctuation of the code weight distribution around the 50% dimming level. Specifically, in the case of a polar encoder with 2048-bit codewords, the percentage of one bits was reported to fluctuate in the range of (42.1875%, 57.8125%).

However, we have found that this fluctuation range can only be achieved when the proportions of 1's and 0's in the input data (before the FEC encoder) are both equal to approximately 50%. Unfortunately, the bit ratio of the input data is unknown beforehand because of the randomness of these data, and this input bit ratio greatly affects the output bit ratio of the FEC encoder. In this paper, we evaluate our proposed method using a worst-case input bit ratio corresponding to 10% zero bits and 90% one bits. A simulation was performed using 10,000 158-bit data frames. If the minimum and maximum bit ratios are included, the real fluctuation

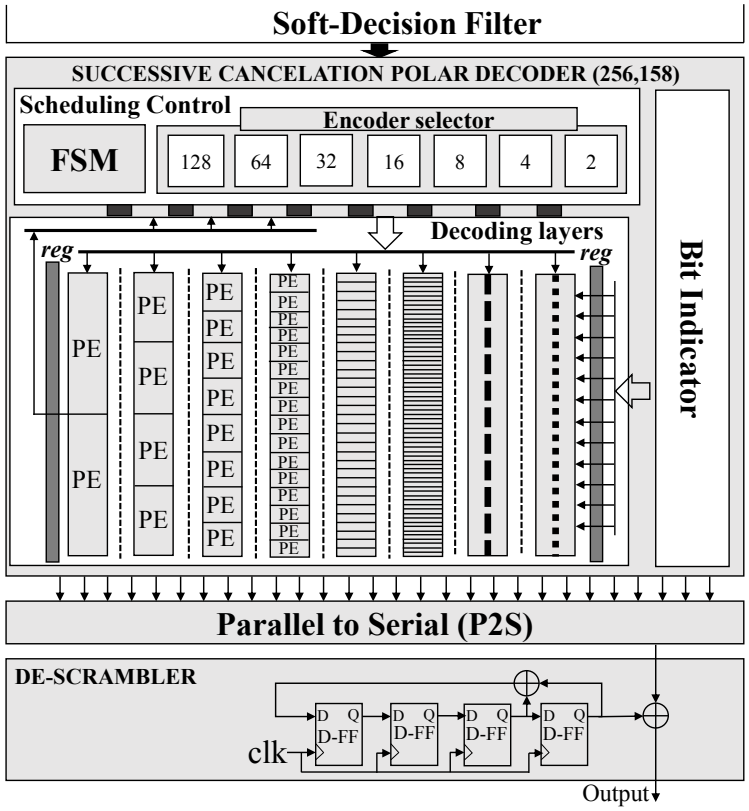

Figure 8. The hardware architecture of proposed non-RLL VLC receiver.

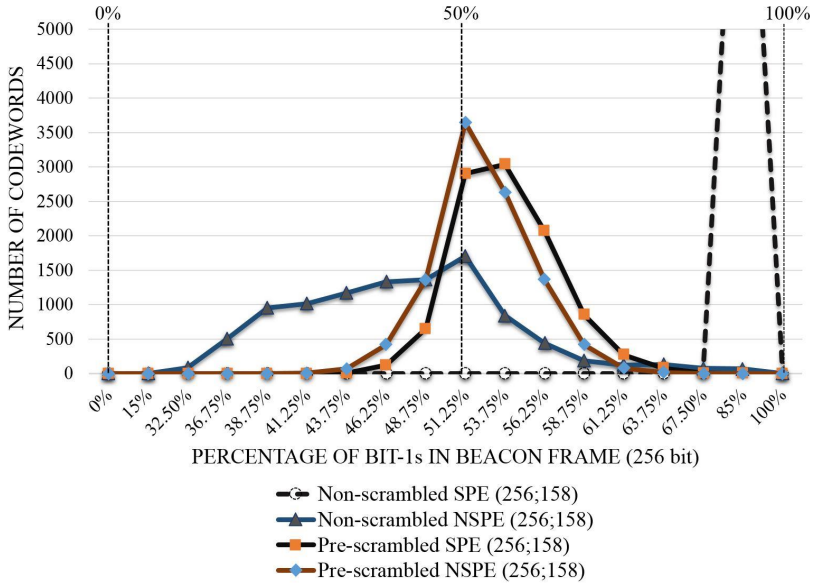

Figure 9. Output bit probability distributions of non-scrambled/ pre-scrambled NSPE and SPE.

range of the output bit probability distribution of a polar encoder with 2048-bit codewords is (41.25%, 61.25%). From the experimental results presented in Figure 9, we can also see that the bit distribution of an NSPE shows a little bit more centralized than that of a SPE regardless of whether pre-scrambling is applied. Especially when a pre-scrambler is not used, the probability distribution of the SPE tends toward 85% one bits because it is greatly affected by the input bit probability distribution. Figure 9 shows the impact of a pre-scrambler on the output bit probability distribution of the NSPE and SPE. Notably, DC balance is not guaranteed in the case of a (256;158) polar code if a pre-scrambler is not applied because the encoder's output bit probability distribution is spread over a large range of percentages (32.5%, 85%). However, when a pre-scrambler is used, the output fluctuation range of the pre-scrambled (256;158) polar encoder is (41.25%, 63.75%), whereas the fluctuation ranges of polar encoders with codeword lengths of 2048 and 1024

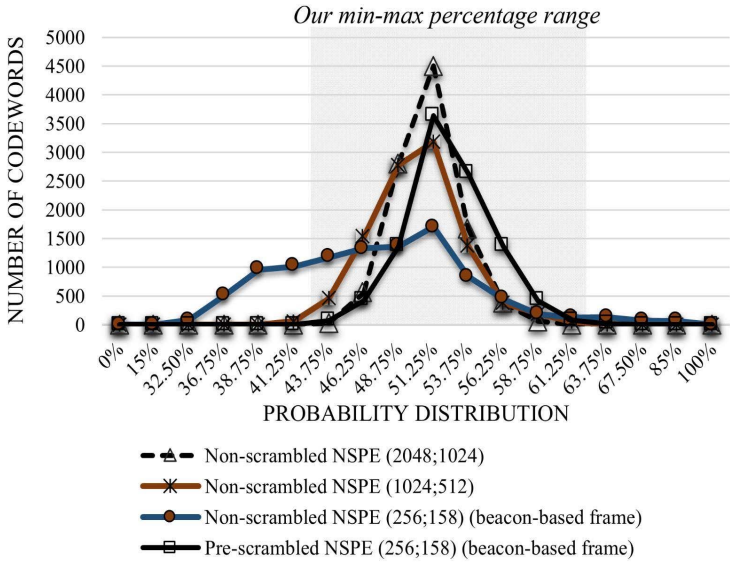

Figure 10. Output bit probability distributions of pre-scrambled and non-scrambled NSPEs with long and short codeword lengths.

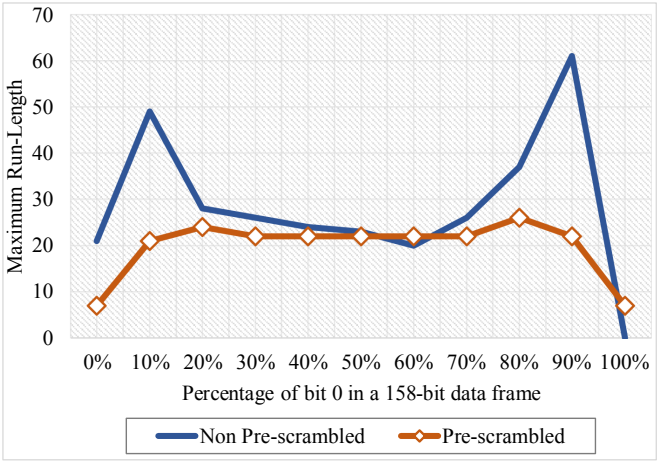

Figure 11. Run-length reduction performance of the pre-scrambled NSPE.

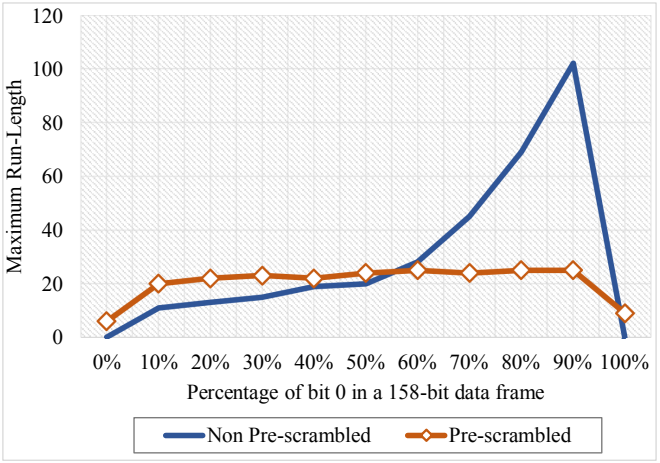

Figure 12. Run-length reduction performance of the pre-scrambled SPE.

are (41.25%, 61.25%) and (38.75%, 67.5%), respectively, which is shown in Figure 10. Thus, pre-scrambling causes the output bit probability distribution of a (256;158) NSPE to be approximately equal to those of (1024;512) and (2048;1024) encoders.

The bit-probability distribution results presented in Figure 9 and Figure 10 demonstrate that a pre-scrambler combined with a Polar encoder is useful for ensuring faster convergence to a centralized output bit probability distribution. Accordingly, DC balance can be guaranteed in VLC-based beacon systems with a short data frame length of 158 bits. Compared with the non-RLL DC-balance solution based only on a polar encoder with 2048-bit codewords presented in [9], the proposed method can achieve the same output bit probability distribution with a codeword length that is shorter by a factor of 8.

Evaluating the flicker mitigation also requires a consideration on run-length of all packets. In the MATLAB simulation model, we have sent 10000 frames with the percentage of bit-0 in each 158-bit data frame changes from 0% to 100%. The results have been presented in graphs at Figure 11 and Figure 12. Accordingly, the maximum run-lengths are reduced remarkably in case of pre-scrambled technique is applied for Polar encoders. Specifically, the maximum run-length reduction gain that NSPE can achieve is 1.9; while an even better effect that SPE has achieved, is the gain of 4.08 when 90% of bit-0 appears in a data frame. About the relationship between maximum run-length and minimum flicker mitigation frequency, we introduce a simple equation (Equation (7)) that may be useful to estimate the minimum transmit frequency. Specifically, F_{minFM} is the minimum frequency that flicker mitigation is guaranteed; *maxRL* is the maximum run-length and *MFTP* is stated around 5 ms [9]. Hence, the minimum frequency that the flicker mitigation in our proposed system is guaranteed is 2.5 Khz, which is still much smaller than the minimum frequency defined in [15].

$$F_{minFM} = \frac{1}{\text{MFTP} \ . \ \text{maxRL}} \tag{7}$$

Table IV
The Proposed Work Compared with Related Works in Key Criteria

Evaluation criteria	Unity-rate [19]	Unary code [20]	Pun, Scram. [22]	Polar code [9]	Prescrambled Polar (this work)
Code-rate	FEC*0.89	0.4, 0.333	0.333	0.5 (FEC*1)	0.617 (FEC*1)
Codeword	1000, 5000	1000, 5000	1024	2048	256
Max run-length	N/A	N/A	N/A	260	27
Bit-0-1 distribution	44%-56% (Dim 50%)	74%-82% (Dim 78%)	48.63% - 51.37%	42.18%-57.81%	41.25%-63.75%

Table V
An Estimation of Complexity Reduction of the Proprosed VLC Receiver Compared with Some Related Works

Computation	Complexity reduction of proposed non-RLL receiver compared with		
	Soft-decoding Manchester-RLL-based [26]	Soft-decoding 4B6B-RLL-based [11,12,14]	Soft-decoding 8B10B-RLL-based (estimation only)
Power	2	2	2
Square root	1	1	1
Exponentiation	1	1	1
Division	2	5	9
Multiplication	2	80	1280
Addition	2	56	896
Logarithm	1	4	8

Table IV summarizes some evaluation results of the flicker mitigation method using the pre-scrambled Polar encoder. Compared with related works, the proposed approach shows advantages in code-rate with an acceptable range of DC balance in short codewords (256 bits). Finally, as mentioned earlier, the max run-length 27 could guarantee the flicker mitigation when the system frequency is more extensive than 2.5 kHz.

5.2 Hardware Implementation Results

Table V shows an estimation of complexity reduction of the proposed VLC receiver compared with related works which based on Soft-decoding Manchester-RLL, Soft-decoding 4B6B-RLL and soft-decoding 8B10B-RLL [13, 14, 18, 18]. It can be seen that, by removing RLL soft-decoding blocks, the complexity of proposed receiver reduces remarkably in term of heavy computation blocks e.g division, multiplication, logarithm, etc. Notably, in cases of 4B6B-RLL-based and 8B10B-RLL-based receivers, by estimation [13, 14, 30], we confirm that hardware implementation of 4B6B-RLL-based and 8B10B-RLL-based are not feasible due to their large number of division, multiplication, addition, and logarithm. Therefore, the proposed non-RLL VLC receivers could be the solution for high-throughput VLC transceivers which could be hardware implemented

The block diagram of the proposed architectures of the VLC transmiter and receiver are presented in Figure 5 and Figure 8. The proposed hardware architecture is described by Verilog HDL language before it is synthesized by Quartus II software. The selected

Table VI
FPGA Synthesys Results of Our VLC Transmitter and Receiver

	Transmitter	**Receiver**
Device	Cyclone IV	Cyclone IV
Model	1200mV 0C	1200mV 0C
Fmax	382.85 Mhz	29.31 Mhz
LE/LUT	1896/114480 (1.65%)	12134/114480 (10.6%)
Registers	1879	3109
Memory bits	0	1152

targeted device is Cyclone IV EP4CE115F29C7 FPGA. FPGA synthesis results of our VLC transmitter and receiver are given in Table VI. It can be seen that the consumed resource of the receiver is much more than the transmitter one. The consumed LE/LUT of our transmitter takes only 1.65% of the Cyclone IV FPGA. This result implies that there are around 60 VLC transmitters can be implemented on the same FPGA. Regarding to this result, we expect that multi-VLC-transmitters could be implemented on one FPGA to reduce the cost and enhance the performance of the VLC system (Section 1.3).

Table VII, VIII summarize the logic resource that components of our transmitter and receiver have consumed. At the transmitter, the Polar encoder is the biggest block which takes around 76% of the whole VLC transmitter. On the other hand, the prescrambler only takes less than 1% resource of the whole transmitter but it provides an effective solution in

Table VII
Resource Summary of Our VLC Transmitter and Its Function Blocks

Instance	Logic Cells	Register	LUT/Reg.LCs
Polar encoder	1437 (160)	1292 (158)	712(75)
Frozen Inserter	158 (158)	158 (158)	712 (149)
Parallel to Serial	259 (259)	258 (258)	193 (193)
Prescrambler	5 (5)	4(4)	5(5)
Serial to Parallel	178 (178)	167 (167)	168 (168)
Total	**1896 (0)**	**1879 (0)**	**946 (0)**

Table VIII
Resource Summary of Our VLC Receiver and Its Function Blocks

Instance	Logic Cells	Register	Mem. bit	LUT/Reg.LCs
Soft-dec. Filter	1341 (1341)	1301 (1301)	1152	1300 (1300)
Polar Decoder	10519 (3192)	1545 (1537)	0	2748 (1522)
Parallel to Serial	267 (267)	258 (258)	0	249 (249)
Descrambler	7 (7)	5 (5)	0	5(5)
Total	**12134 (0)**	**3109 (0)**	**1152**	**4302 (0)**

Table IX
Logic-Resource Consumption of the Proprosed VLC Transmitter Compared with Related Works

	Manchester-based	4B6B-based	Proposed
Model	Cyclone IV	Cyclone IV	Cyclone IV
Code length	256	256	256
FEC	Polar code	Polar code	Polar code
Code rate	0.308	0.411	0.617
Logic Cells	1825	1855	1896
Memory bits	53	6201	0

Table X
ASIC Synthesis Results of Our VLC Transmitter and Receiver

	Transmitter	Receiver
Technology [nm]	180	180
Voltage [V]	1.8	1.8
Area [μm^2]	48761.39	573724.56
Frequency [Mhz]	25	25
Power [mW]	1.3137	3.5022
Throughput [Mb/s]	15.38	16.58
Energy-per-bit [pJ/b]	85.42	211.2
Hardware Efficiency [$Mb/s/mm^2$]	315.41	28.75
Latency [$clocks$]	160	386

centralizing bit-probability distribution (Section 5.1). At the receiver, the Polar decoder block is the most heavy one. Specifically, it takes more than 85% resource of our receiver. Whereas, the soft-decision filter occupies around 11%, and the descrambler only takes an unnoticeable amount of logic cells. The maximum frequency of the VLC transmitter can be up to more than 382 Mhz because the polar encoder is created mostly from modulo-2 computations which are simple elements. On the contrary, the receiver's maximum frequency is reported at 29.31 Mhz. The reason for this relatively low frequency is as we mentioned in Section 4.2.2; due to the nature of VLC-based beacon systems, high-throughput is not a high-priority criteria in VLSI architecture design. Therefore, we have implemented a architecture based on combinational logic for the network of PEs; hence, this causes an increase in delay of PEs-network and a deduction of frequency. Moreover, the synthesis results of consumed LEs/LUTs of transmitter and receiver are strongly affected by the code-length of Polar encoder/decoder. Specifically, We have noticed that the amount of consumed LEs/LUTs almost duplicate when the code-length increase 2 times. Table X introduces some ASIC synthesis results of our VLC transmitter and receiver. Specifically, we have utilized the Synopsys' Design Compiler RTL synthesis tool in which the VDEC's Rohm technology library 180nm is selected. Besides results of power consumption and area are reported, we also evaluate the throughput, energy-per-bit and hardware efficiency of implemented transmitter/receiver based on equations given in this paper's appendix (8, 9, 10) [31].

Table IX shows that the proposed VLC transmitter does not use any memory bits in logic synthesis compared with related works. Besides, Table V shows a complexity reduction of the proposed receiver compared with related works. Due to not using soft-decoding for any RLL codes, our works could reduce remarkably heavy computation efforts such as multiplication, division, logarithm, etc., which had been a big obstacle in hardware implementation of soft-decoding-based VLC receiver.

5.3 Bit Error Rate (BER) and Frame Error Rate (FER) Performances

Figure 13 shows the BER performances of our proposed VLC system in which both systematic and non-systematic Polar codes are applied to evaluate the BER

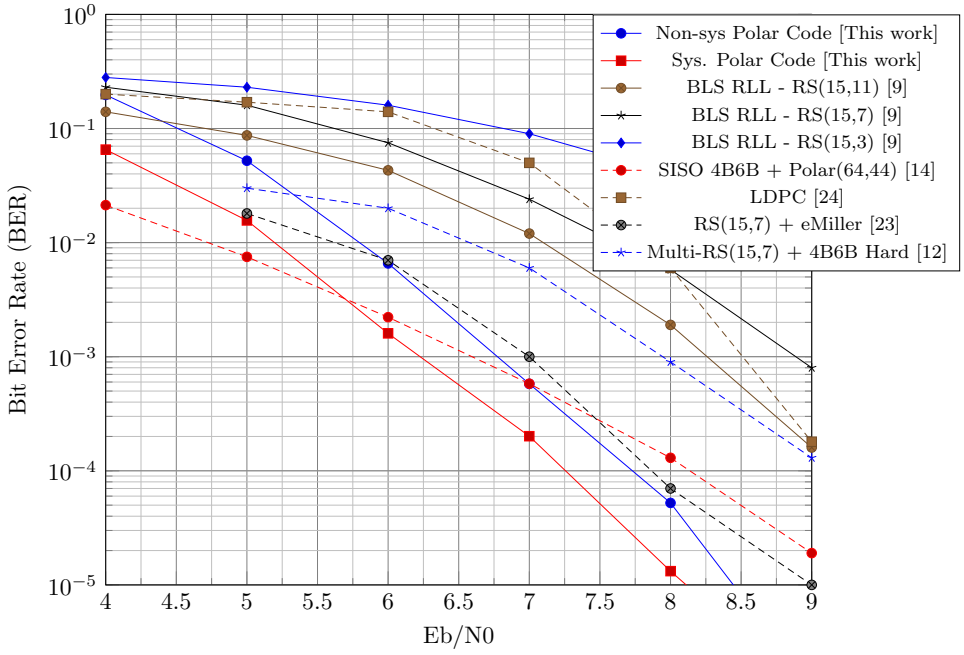

Figure 13. BER performances of the proposed VLC system with some comparisons in real VLC-AWGN channel.

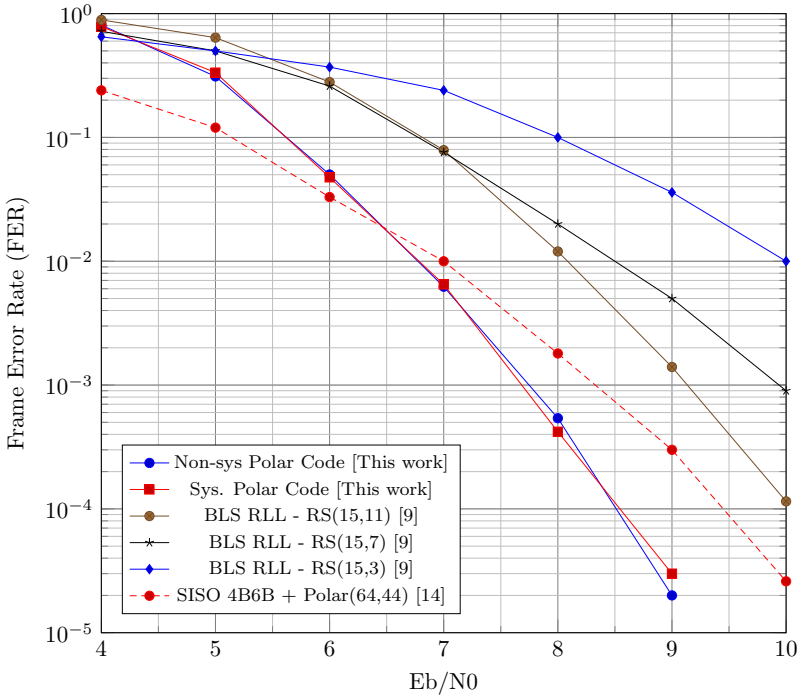

Figure 14. FER performances of the proposed VLC system and some related works in real VLC-AWGN channel.

performances. We have selected some typical joint FEC-RLL and non-RLL FEC solutions for comparison. It can be seen that the BER performances of our proposed system outperform current related works. Specifically, Figure 13 shows that at a code-rate = 0.62, our non-RLL Polar-code-based system outperforms RS-code-based ones at code-rates 0.49 (11/15 * 4/6), 0.31 (7/15 * 4/6) and 0.13 (15/3 * 4/6) which are mentioned in [11, 14]. Also, in Figure 13, we also put BER performances of other related works mentioned in [14, 16, 17, 24] into the same graph with our BER performance lines. It can also be noticed that, our prescrambled non-RLL Polar code-based solutions have preeminent BER performances although their humble code-rates compared with the related works. Furthermore, an evaluation of frame error rate (FER) has been presented in Figure 14 in which our non-RLL solutions also surpass related works introduced in [11, 14, 30]. However, although systematic Polar decoder always shows a better BER performance than the non-systematic decoder does; the FER performance of these two decoders are always equal in all cases. Actually, this is not a strange discovery cause it has been mention in previous systematic Polar decoder work [32].

6 Conclusions

We have introduced a non-RLL flicker mitigation solution which consists of a pre-scrambler based on a simple generating polynomial combined with a Polar encoder. The proposed method has a centralized bit probability distribution with the distribution range is determined in (43.75% - 63.75%). Moreover, the maximum run-length is reduced up to 4.08 times when pre-scrambler is applied with a SPE; and up to 1.9 times when it is applied with a NSPE. Therefore, DC-balance can be maintained even with the short data frames used in VLC-based beacon systems. Moreover, the non-RLL nature of the proposal reduces the complexity of both VLC transmitter/receiver with great improvements on information code-rate. Besides, we have introduced a soft-decision filter which can help the soft-decoding of polar code is implemented in real VLC receiver prototypes to enhance the error-correction performance. As a result, BER and FER performances of the proposed system have outperformed current approaches while remaining a good code-rate (0.62). In addition, we have introduced a couple of hardware architectures for the proposed non-RLL VLC transmitter and receiver which their FPGA and ASIC synthesis results are given in details.

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Appendix

$$\text{Thoughput [b/s]} = \frac{N \text{ [b]}}{D_N \text{ [sec]}} \tag{8}$$

$$\text{Energy-per-bit [J/b]} = \frac{\text{Power [W]}}{\text{Thoughput [b/s]}} \tag{9}$$

$$\text{Hardware Efficiency [b/s/}m^2\text{]} = \frac{\text{Thoughput [b/s]}}{\text{Area } [m^2]} \tag{10}$$

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