

*Invited Article*

# Integrated On-Silicon and On-glass Antennas for mm-Wave Applications

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**Abstract**– The paper presents several integrated high frequency antenna prototypes based on Silicon (Si) CMOS and on-glass technologies for millimeter-wave (mm-wave) applications. An on-chip loop antenna and dipole radiator are presented. In addition, a wide-band dipole-patch antenna design for the range of 74 – 104 GHz is integrated into a CMOS chip with an on-chip pulse generator. In addition, an implementation of a fully on-Silicon antenna array integrated with a timed-array transmitter is introduced. To control the beam-forming of this array, a digital time adjustment circuit is integrated together with the antenna array. Simulated and measured data including return loss, and radiation patterns are presented. This paper also introduces an on-glass antenna prototypes fabricated on quartz substrate. The on-glass antenna is to demonstrate for handset or automobile’s windshield/windows applications where radio waves could be transmitted and received from various directions. The results show several compact antenna candidates integrated on both Si and quartz substrates towards mm-Wave/sub-mm-Wave sensing and communication applications.

**Keywords**– antenna, mm-wave, on-chip, quartz, on-glass, integrated, array, CMOS, BiCMOS, calibration

## 1 INTRODUCTION

Nowadays, the evolution to high-speed cellular communication requires a completed integration of a mm-wave/sub-mm-wave system including passive components, active circuits, and even multiple antennas into a small chip. Realizing such integrated antenna system requires significant challenges such as form factor, low-power consumption, wide bandwidth, etc. for RF front end. Integrated antenna bandwidth is very important for the whole mm-wave system which requires critical broadband and high Gbps data rates in 5G applications such as high resolution radar imaging or cellular communication. In recent years there has been an increasing interest in mm-wave/sub-mm-wave antennas design, integration, and measurement. Although antenna integration confronts losses from the low-resistivity of Si-substrate and other interference [1], antenna array implementation enhances radiated power, reduce interconnections between on-chip RF circuit and off-chip antennas, and provides a controllability of the array’s beam-forming for communication, sensing and imaging purposes

The smaller wavelength at millimeter-wave frequency leads to higher free-space path loss; however, it also facilitates small-size high-gain antenna design, which can be used to compensate for the loss. By using Silicon technologies, completely integrated high frequency systems including inductors, capacitors, antennas and other RF components can be integrated in a

very small area for getting high system performance and for reducing significantly size, cost and power. Antenna integration with its integrated system is an attractive topic due to the benefits of scaling and the possibility of integrating the digital backbone with the RF front-end. The specific features of CMOS technology process and its plenty of process design rules such as metal path spacing, number of metal layers, angle for metal path, and metal density etc. limit antenna and antenna array categories to be integrated. On-chip antenna implementation is considered carefully based not only on antenna’s size, operating frequency and specific applications but also on the fabrication process.

In addition, this paper will deliberate some antenna candidates to be integrated into a chip and form an integrated antenna array. Several constraints related to on-chip antenna array implementation will be presented. From the analysis of these requirements for integrating antenna array into a Si-based chip, designers can decide suitable array’s parameters and necessary design trade-off for mm-wave applications.

In this paper, several challenges for integrating antennas into a chip are discussed. In addition, the paper will review several on-chip antenna design on Si-substrate and also presents our latest results of on-glass antenna design and measurement. The article is organized as follows. Section 2 introduces several challenges for antenna integration in mm-wave frequency regime. In Section 3, on-Si antenna and antenna array implementation are presented. On-glass antenna fabrication

and measurement are shown in Section 4. The paper conclusions are drawn in Section 5.

## 2 CHALLENGES FOR ANTENNA INTEGRATION IN HIGH FREQUENCIES

There are several important factors to determine a suitable antenna operating in mm-wave frequency range to be integrated into a chip such as operating frequency, bandwidth  $B$ , directivity, gain, half-power beam-width (HPBW) and radiation efficiency. However, the mostly important parameters for antenna designers are  $B$  and efficiency. In mm-wave frequencies, antenna performance at center frequency  $f_0$  depends on relative bandwidth  $B/f_0$  and the antenna size becomes small as its size is often proportional with the wavelength,  $\lambda$ , about  $\lambda/2$  or  $\lambda/4$ , [1]. The mm-wave regime corresponds to a frequency range between 30 to 300 GHz or to correspond to free space wavelengths between 10 and 1 mm. Therefore, antenna integration into a chip is possible in mm-wave frequency regime but with many challenges not only for antenna bandwidth, efficiency but also for antenna size, geometry, losses, and others.

There are various types of antennas for many applications with different shapes and sizes as illustrated in Figure 1 such as dipole, patch, parabolic, horn, etc. However, there are only several antenna types that can be integrated into a chip. In a Si-technology-based integrated circuit like CMOS or BiCMOS, there are plenty of process design rules, such as spacing between metals, metal width and thickness, angle for metal path, or antenna rules, etc. and that limits the on-chip antenna category to be designed. For example, it is impossible to implement on-chip horn antennas or parabolic shaped antennas because their shape is incompatible with standard CMOS process' metal planar structures. Although there are many general shapes of micro-strip patch antennas, only a few shapes are suitable for integrating into a chip, such as square, rectangular, dipole, circular, triangle, etc.

For integrating a loop antenna into a chip, a loop antenna in mm-wave frequencies can have small size due to the corresponding wavelength. Several integrated loop antennas are successfully integrated and located at the perimeter of the chip [2, 3]. In several applications requiring far-field radiations perpendicularly to the chip's surface loop antenna may not be a compatible candidate to be integrated into a single chip. The maximum radiated direction or the directivity of loop antennas is on the same horizontal plane of the loop and hence the chip's bonding-wires and package can resist, scatter, or even degrade the main radiation beam.

Integrating an antenna into a Si chip also confronts losses from the low-resistivity of Si-substrate and other interference. The back-lobe of the far-field radiation in case of no ground plane is much larger than the front-lobe and most of the antenna's power radiates backward to the Si-substrate, while the on-chip with-ground-plane antenna radiates its power to the air and

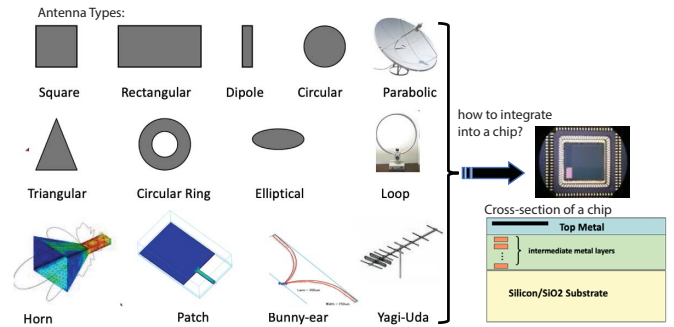


Figure 1. Antenna types and challenges to integrate into a chip.

has no back-lobe [4]. Therefore, the decision for an integrated antenna will be made based on its suitable shape, form-factor, termination configuration, and radiation pattern.

Moreover, the substrate material underneath integrated antennas poses another challenges to be considered. In Si technologies, the Si substrate has a high permittivity and that reduces on-chip antenna dimension which is inversely proportional to the square root of the effective permittivity [1]. However, the larger permittivity of the substrate (for example,  $\epsilon = 11.7$ ) compared with air's permittivity ( $\epsilon = 1$ ) causes the back-lobe of the on-chip antenna to be larger than the front-lobe [4] and most of its radiated power comes out to the Si-substrate. In addition, the resistivity of the Si-substrate is low and hence causes high loss and low antenna efficiency. The solution to avoid the back-lobe radiation of an on-chip antenna is to additionally place a metallic ground (GND) plane or mesh underneath the antenna. This solution may reduce the back-lobe radiation of the antenna, however requires much effort to design the GND plane to meet the constraints imposed by the process technology, especially for density rules, electrical rule check (ERC), and design rule checking (DRC) errors. Furthermore, the substrate beneath on-chip antennas may limit the antenna directivity. To improve directivity, back-side removal methods such as etching the substrate underneath the antenna can be applied with additional costs [5].

The effect of packaging methods on integrated antennas needs to be considered. Packaging works include molding, shielding, and bonding. Bonding-wires connected to the antenna inputs can be in several millimeters in length and that will introduce considerable parasitic inductance to the antenna input as in mm-wave frequency regime, the wavelength values varies between 1 and 10 mm in the air and are comparable with these bonding-wires. The additional parasitic inductance can corrupt the impedance matching at the antenna input and hence degrade the antenna performance. To avoid such effects of long bonding wires, wire bond compensation techniques are used [6] or flip-chip packaging techniques can be applied. With the use of solder balls, flip-chip packaging technique significantly reduces inductance connected to antenna inputs [7–9]. Furthermore, the chip in which antennas are integrated can be placed into a cavity by a

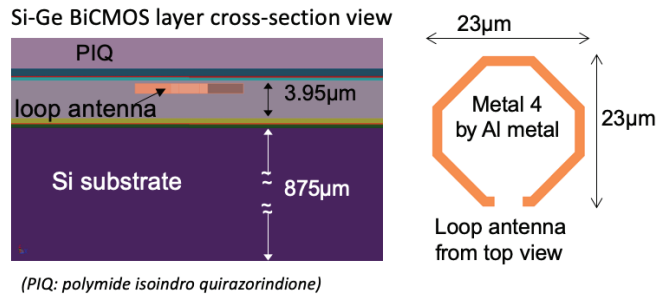


Figure 2. Loop antenna is operated as an inductor and integrated into a Si-Ge BiCMOS chip [10].

packaging method. However, this cavity may be closed by a lid which will limit the antenna's radiation pattern.

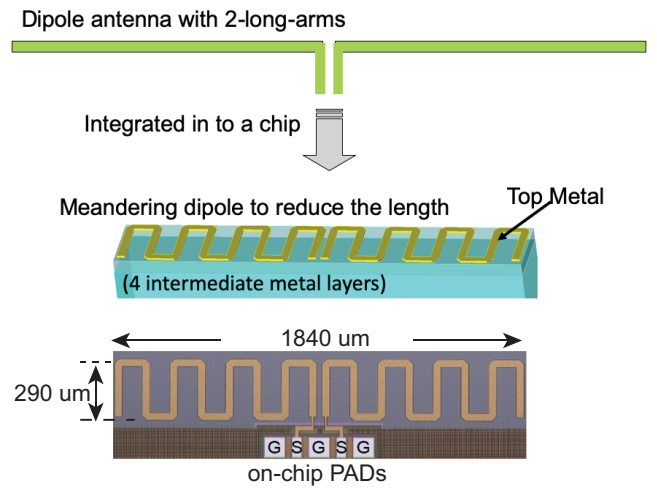
### 3 ON-SILICON ANTENNA AND ARRAY DESIGN

There are several commonly used antenna types: slot antenna, loop antenna, micro-strip patch antenna, or dipole antenna that can be integrated into a chip. The high permittivity of Si materials in CMOS technology enables to reduce on-chip antenna dimension which is inversely proportional to the square root of the effective permittivity of the surrounding environment. However, the usage of low resistivity Si substrate causes high loss and low antenna efficiency. A loop antenna is designed to employ its impedance for forming an R-L-C generating damping circuit and then is fabricated in a 2.5-V 0.25- $\mu\text{m}$  4-metal-layer SiGe BiCMOS process [10]. The loop antenna is small and located on the top metal as shown in Figure 2. Its resistance value is small, 3  $\Omega$ , and hence the radiation may not be enough for the target of mm-wave sensing application. The challenge coming from the small resistance value of the loop antenna can be solved by using a large loop radiator array to form high radiating power and beam-forming capabilities. However, for the loop antenna choice, the maximum radiated direction of a loop antenna is the main challenge as it is on the antenna's plane and also on the chip surface whose bonding-wires and package can resist and scatter the main radiation beam.

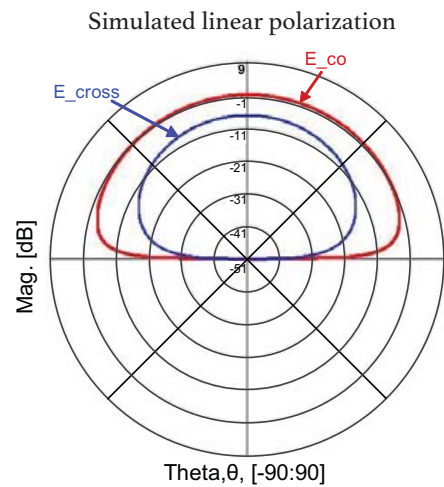
Patch and dipole antennas offer different radiation directions and have several advantages compared with loop antennas. Their maximum radiations are mainly perpendicular to the plane of antennas. Patch antenna can eliminate back lobe due to the backside ground plane; which offers electric-magnetic benefits for forming antenna array. However, it is just suitable for unbalanced feeding device; and requires a large metallic plane underneath which can violate layout design rules in Silicon technologies. In contrast, dipole antenna requires balanced feeding termination and can overcome process design rules. Nevertheless, dipole antenna has radiated back lobes and requires long arms as shown in Figure 3.

#### 3.1 On-chip Dipole Antenna

Figure 3 presents a solution to shorten the long arm requirement of integrated dipole antenna [11]. The



(a) Dipole antenna integration into a Si chip in a meandering shape to reduce long arms



(b) Simulation and measurement results

Figure 3. Integrated meandering dipole antenna on 180 nm CMOS process and simulation results.

dipole antenna's arms are in meandering shape and placed on the top metal of a 180 nm CMOS process technology. As dipole terminal is balanced, a differential GSGSG pad is added for probing measurement. Figure 3(b) shows simulated and measured results of its linear polarization and S11. A de-embedding method using "open", "short", and "through" patterns is applied in the S-parameter measurement to remove substrate coupling and contact effects. However, the measured S11 is positive at around the frequency range from 15–24 GHz and this phenomenon may be from the reflection and the coupling of the probe tips and the dipole. The dipole is also integrated with a pulse generator (PG) into a chip for time-domain measurement.

The measurement setup, depicted in Figure 5(a), employs a 10–15 GHz 20-dB standard horn antenna, which is placed perpendicular to the chip at a distance of 38 mm is connected to a sampling oscilloscope. The received pulse signal is 1.1 mV peak-peak (p-p) with the frequency response is 9–11 GHz, good matching with the dipole's S11.

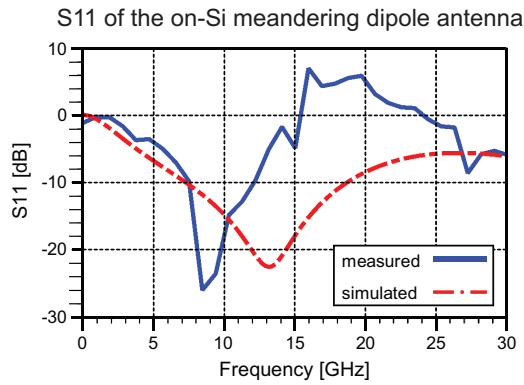


Figure 4. S11 simulation and measurement results of the on-Si dipole antenna.

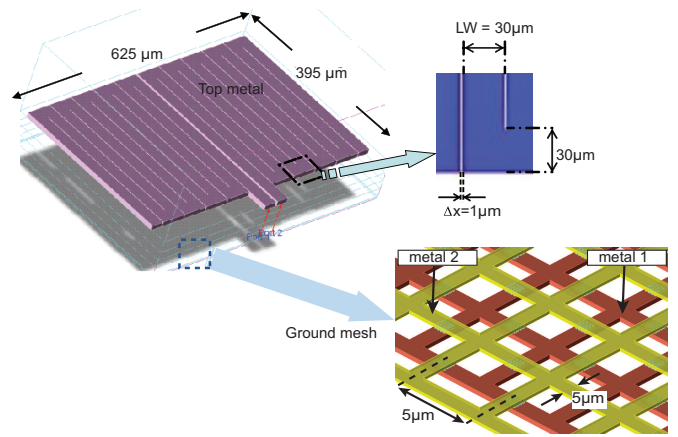
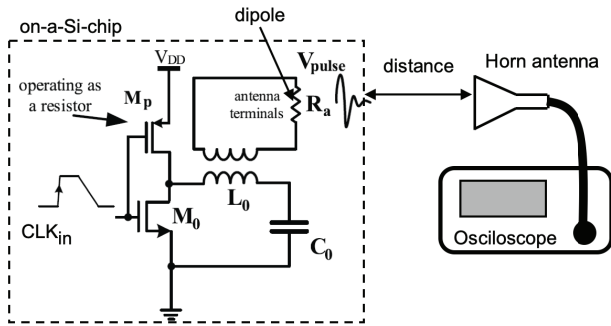
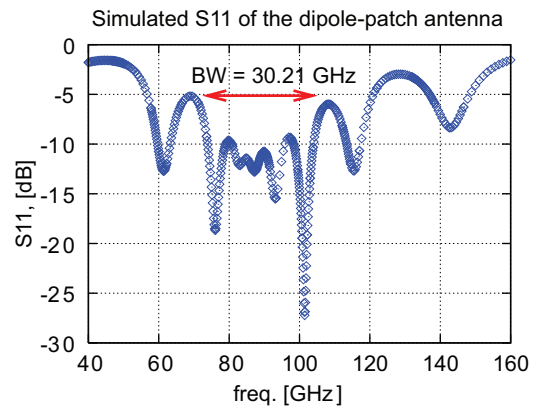


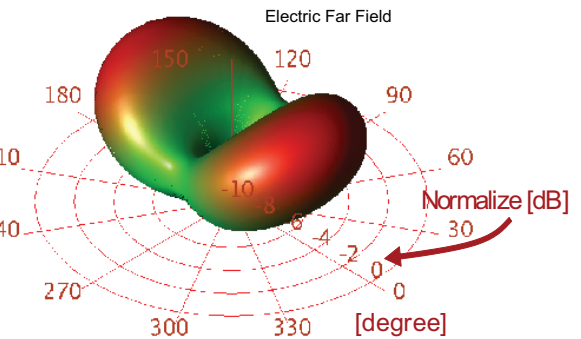
Figure 6. Dipole-patch antenna integration into a Si chip with a GND mesh.



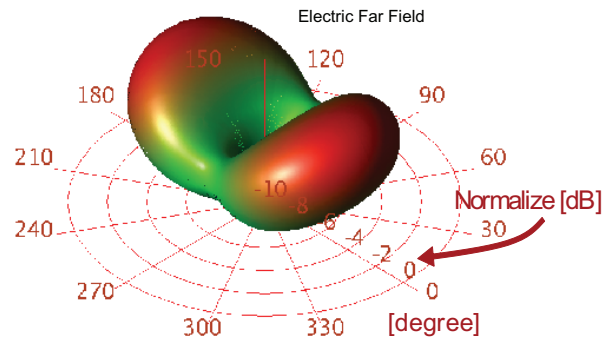
(a) Measurement setup using a standard horn antenna placed at a distance from the chip



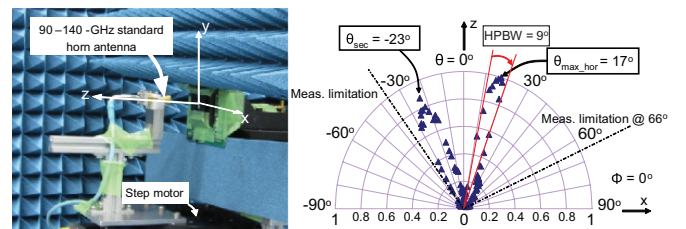
(b) Measured pulse waveform at the output of the standard horn antenna results



(a) Simulation of S11 of the antenna results



(b) Simulation of 3D radiation pattern results



(c) Measurement setup and radiation pattern results

Figure 7. Integrated meandering dipole antenna on 65 nm CMOS process and measurement results.

### 3.2 On-chip Dipole-Patch Antenna with Ground Mesh

Most of the radiated power of an integrated dipole antenna comes out to the Si-substrate due to the large permittivity of silicon substrate ( $\epsilon_{eff} = 11.7$ ) compared with air permittivity ( $\epsilon_{air} = 1$ ). This back-lobe radiation phenomenon can be avoided by using a back ground (GND) plane underneath the dipole or by using a patch antenna. A ground plane or ground mesh placed underneath the dipole radiator is to reflect radiated power back to the air to avoid such undesired big back

radiation. The metal ground plane can be located in the lowest metal layer while the antenna is at the topmost metal layer. Figure 7 shows an integrated antenna with a mesh GND plane in our previous work [4].

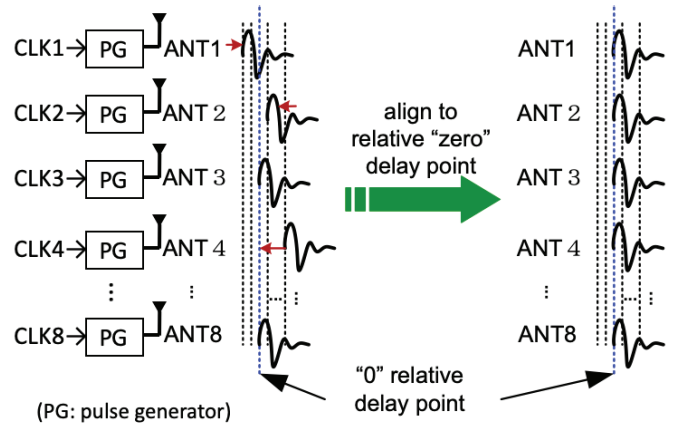
This antenna is a combination of dipole and patch radiator types and is integrated into a 65nm CMOS process chip. To avoid metallic density rules of the process, the ground mesh underneath the on-chip antenna is made by using metal-1 and metal-2 layers. In addition, the mesh is used to shield active layers from antenna radiation from top-metal layer based on calculation from [12]. The operating bandwidth of the antenna is 74–104 GHz in simulation as shown in Figure 7(a). Electromagnetic simulation results of the on-chip antenna including radiation and polarization patterns are presented. In addition, the dipole-patch antenna is integrated with a PG into a chip to characterize its radiation patterns. The measurement setup employs a 90–140 GHz standard horn antenna attached to a mm-wave Schottky diode as a detector. The PG output is connected to the antenna by an on-chip transformer. Measured radiation patterns as presented in Figure 7(c) show two main beams of the antenna, matching with the simulation one.

### 3.3 Integrated Antenna Array with On-chip Skew Calibration Technique

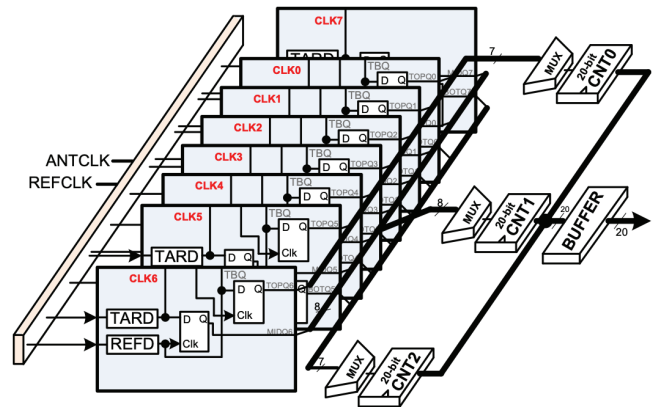
Due to the small form-factor of integrated antennas as well as the chip-package limitation, radiation power of a single integrated antenna might not be high nor sufficient enough for some practical applications. To enhance the required radiation and system performance multiple antenna elements can be integrated into a chip to form an antenna array. Such a number of antenna elements or antenna array can provide a beam-forming to focus the radiation signal towards a specific receiving device with controllable beam angles and beam-width, rather than having the signal spread in wide directions from a single element. Beam-forming and beam-scanning are performed by phasing the feed to each element of an array so that signals received or transmitted from all elements will be in phase in a particular direction. In mm-wave frequency regime, phase control and propagation delay of the signals required for beamformability are in the range of sub nanoseconds or even picoseconds. Therefore, integrated antenna array design in mm-wave frequencies gets more challenges and issues than single radiator integration one.

One of the challenges for integrating an mm-wave antenna array into a single chip is to calibrate the propagation delay of array elements. Phase or time-delay differences between array elements are very important for beam-forming control. However, process variations in semiconductor including skews in time domain. Depending on the fabrication process, the delay or skew variations can be up to several tens of picoseconds and that can cause inability to control the antenna array for beam-forming and beam-scanning which require timing calibration for each array elements.

Figure 8(a) illustrates a functional block diagram of an antenna array transmitter including pulse delay monitor and control unit, on-chip jitter measuring circuit, and debug block. This transmitter is integrated into a 2-mm×4-mm chip by using a 65-nm CMOS



(a) Calibration idea for antenna Array



(b) On-chip pulse skew calibration diagram for array antenna clock inputs.

Figure 8. On-chip pulse skew calibration diagram for array antenna.

process. An 8 element dipole antenna array with time delay monitor & control circuit, meandering dipole antenna, shock wave generator with this antenna and an on-chip jitter measuring circuit are integrated in this chip for mm-wave shock wave transmitter system.

Each of dipole antenna is fed to output terminals of a shock wave generator or pulse generator (PG) through a transformer. The PG is implemented by employing serial RLC circuit principle. In this chip, the PG is designed to obtain output pulse with center frequency of 100-GHz and minimum pulse delay of 1-ps. An 8-digitally programmable delay circuit supplies an ability of pulse delay adjustment with 7-bit data input. Moreover, an on-chip jitter measuring circuit is added to the circuit in order to monitor and adjust the pulse delay as well as jitters by observing 20-bit data output values. The timed delay monitoring and controlling circuit for the whole array system is also fabricated.

The idea to adjust pulse delays between antenna elements is developed from the wave to manually tune guitar’s string without tuner.

Figure 8 describes the inverter chain buffer and the  $i^{th}$  pulse generator (PG) which employs the operation principle of serial RLC circuit,  $i = 0 \dots 7$ . After changing several values of  $Q_{Ni}$ 's  $W/L$  ratio as the same procedure in Section 3.1 and based on estimation of power consumption, peak-peak pulse output, generated pulse

frequency, and chip area, a ratio of  $W/L = 8 \times 100\text{-}\mu\text{m}/60\text{-nm}$  is determined for  $Q_{Ni}$  and a small PMOS size of  $W/L = 2\text{-}\mu\text{m}/100\text{-nm}$  is chosen for  $Q_{Pi}$ . The source (S) terminal of NMOS  $N_{M3}$  is not shorted to ground but connected to output terminal,  $V_{VARi}$  of a digitally programmable delay circuit (DPDC) in order to adjust delays of clock signal  $V_{inQi}$  and also of pulse output signal at antenna's terminal.

A simple binary-weighted current-steering DAC (Digital to Analog Converter) is used for controlling the current of variable delay elements which only affects driving current of the third inverter in Figure 8(b) to achieve precise resolution such as sub-picoseconds. Figure 8(b) presents a detailed diagram of RESC and a target variable delay line including a 7-bit DPDC and 4-inverter delay chain. By varying input vectors of DPDC, the current  $I_{VARi}$  is changed and hence output pulse delays are achieved. This ability to adjust pulse delays is the requirement of wide-band antenna array operation principle for pulse beam-forming and steering. Simulated result of the target variable delay line characteristics vs. input delay code in which minimum differential delay can be achieved at 0.1 ps.

We introduced an on-chip calibration method for antenna array as illustrated in Figure 8(a) to perform an on-chip pulse alignment for all eight array's elements which are fed into the outputs of 8 PGs [13, 14]. Eight clocks of antennas are distributed by a clock-tree layout to one clock input, ANTCLK. To perform the skew calibration, another clock is used as a reference one, REFCLK. The principle of the skew calibration is based on the operating property of D-flip flop (F/F) when swapping two terminal CLK and D inputs of D-F/F then sweeping the delay of the other.

Feeding line network is usually used to distribute signals to each antenna element for the desired beam-forming direction. For wide-band antenna array, clock tree structure, so-called feeding line clock network, is conventionally employed to ensure equally distributed micro-trip or transmission line paths to each antenna block. However, in high frequency-based antenna arrays, clock tree distribution method generates jitters and skew at terminals of target antenna blocks and hence needs skew measurement and adjustment circuits or equipment. While jitters and skew measurements require special equipment with large output drivers, skew adjustments in some cases cannot be re-corrected after fabrication.

At first, outputs of two target/reference VDLs are connected to D input and clock input of a D-FF, respectively, and then a Cumulative Distribution Function, CDF1, is obtained by scanning input code values of the reference VDL. Next, output of the target VDL is changed to clock input of a D-FF while output of the reference VDL is connected to the same D-FF's data input. Another CDF, CDF0 is drawn by sweep the input code values. From the combination of these two functions, CDF0 and CDF1, two D-FFs' setup times is measured. If two D-FFs are same and symmetrical in structure, D-FF's setup time measurement can be achieved just by dividing the two D-FFs' setup timing by 2.

3D Far-field Simulation of the Array Antenna

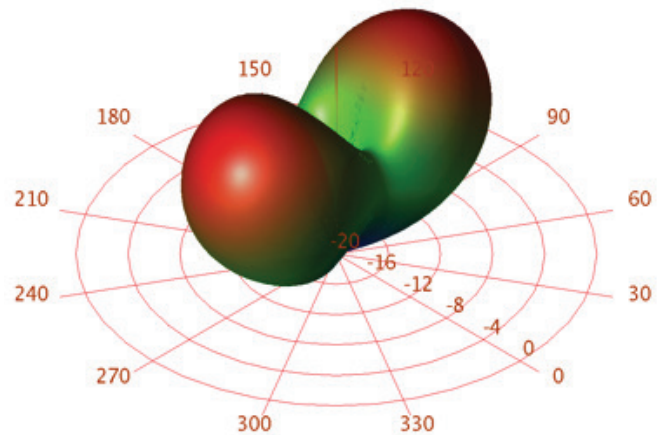
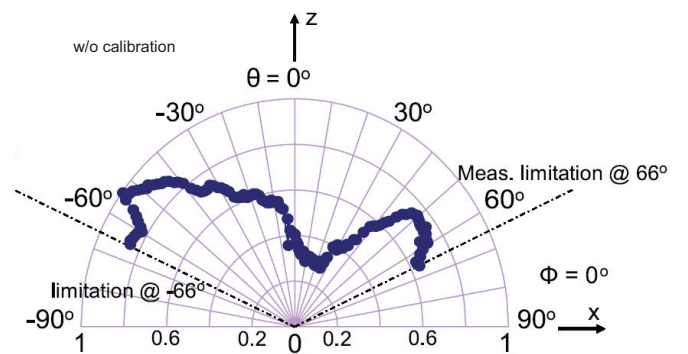
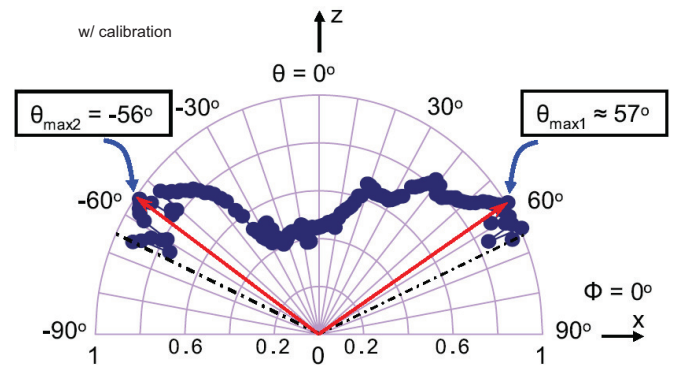


Figure 9. Far field simulation of the 8-element array antenna in the case no phase difference between elements.



(a) Radiation measurement results without skew calibration



(b) Radiation measurement results with skew calibration

Figure 10. Radiation simulation and measurement results with and without on-chip pulse calibration.

The integrated 8-antenna array transmitter with 8 pulse generators and a pulse delay system to adjust on-chip skew and pulse-delay was performed. The transmitter is an on-chip array of 8-dipole antennas with programmable pulse-delay monitoring and controlling system. A digitally controllable pulse-array circuit is integrated together with the antenna array to adjust on-chip relative pulses. Measured radiation pattern results illustrate beam-forming angles obtained versus input codes as shown in Figure 10. This result demonstrates that the antenna array transmitter can be digitally controlled for active imaging in medical diagnosis applications.

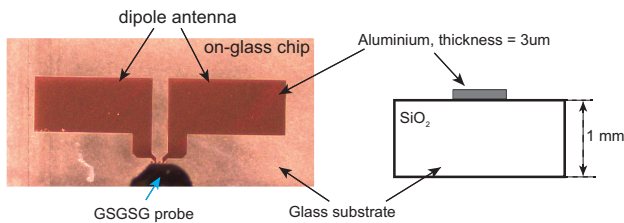


Figure 11. On-glass dipole antenna cross-section.

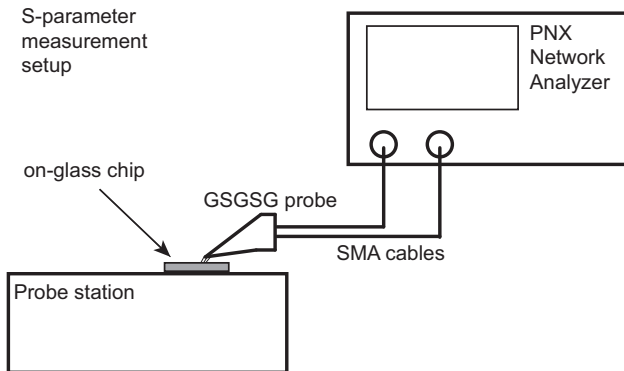


Figure 12. On-glass dipole antenna probing measurement.

#### 4 ON-GLASS ANTENNA DESIGN AND FABRICATION

For antenna designers, antenna substrate is a key parameter to consider because the substrate material determines the antenna bandwidth, antenna loss, the back reflector, back-lobe radiation, and the isolation mean between the antenna, feeder, and other RF related components. In several applications where transmits and receives through antenna substrate are re

To avoid the back-lobe radiation at large permittivity Si-substrates, quartz or glass materials are used for the antenna substrate. In addition, in some applications where radio waves need to be transmitted and received from various directions, on-glass antenna is applicable and suitable. This paper also introduces an on-glass antenna prototypes fabricated on quartz substrates as shown in Figure 11. The antenna is in dipole shape with thick and large arms. A GSGSG pad is attached to the antenna terminals for probing measurement. The probe lands to the GSGSG pad and connected to an Agilent N5247A Network Analyzer to measure S11 values. The measured operating frequency center of the antenna is at 14 GHz. The on-glass antenna is to demonstrate for handset or automobile's windshield/windows applications.

#### 5 CONCLUSION

This paper presents several integrated antenna designs and measurements in both Si-substrate and glass substrate. Experimental results show that the proposed on-chip transceiver has an ability of digital transmitted-pulse calibration and detection of beam-forming pulses not only for communications but also active imaging or diagnosis applications.

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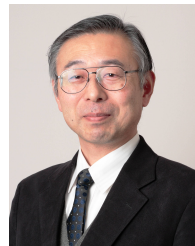
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